

ADG451/ADG452/ADG453
FEATURES

Low On Resistance (4 Ω)
On Resistance Flatness 0.2 Ω
44 V Supply Maximum Ratings
±15 V Analog Signal Range
Fully Specified @ ±5 V, +12 V, ±15 V
Ultralow Power Dissipation (18 μW)
ESD 2 kV
Continuous Current 100 mA
Fast Switching Times
 t_{ON} 70 ns
 t_{OFF} 60 ns
TTL/CMOS Compatible
Pin Compatible Upgrade for ADG411/ADG412/ADG413
and ADG431/ADG432/ADG433

APPLICATIONS

Relay Replacement
Audio and Video Switching
Automatic Test Equipment
Precision Data Acquisition
Battery Powered Systems
Sample Hold Systems
Communication Systems
PBX, PABX Systems
Avionics

GENERAL DESCRIPTION

The ADG451, ADG452 and ADG453 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

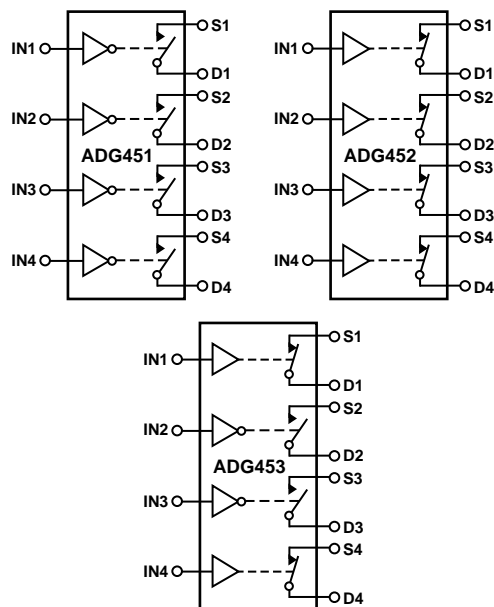
The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG451, ADG452 and ADG453 contain four independent single-pole/single-throw (SPST) switches. The ADG451 and ADG452 differ only in that the digital control logic is inverted. The ADG451 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG452. The ADG453 has two switches with digital control logic similar to that of the ADG451 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked.

REV. A

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FUNCTIONAL BLOCK DIAGRAMS

SWITCHES SHOWN FOR A LOGIC "1" INPUT

The ADG453 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Low R_{ON} (5 Ω max)
2. Ultralow Power Dissipation
3. Extended Signal Range
The ADG451, ADG452 and ADG453 are fabricated on an enhanced LC²MOS process giving an increased signal range that fully extends to the supply rails.
4. Break-Before-Make Switching
This prevents channel shorting when the switches are configured as a multiplexer. (ADG453 only.)
5. Single Supply Operation
For applications where the analog signal is unipolar, the ADG451, ADG452 and ADG453 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5.0 V.
6. Dual Supply Operation
For applications where the analog signal is bipolar, the ADG451, ADG452 and ADG453 can be operated from a dual power supply ranging from ±4.5 V to ±20 V.

ADG451/ADG452/ADG453–SPECIFICATIONS¹

Dual Supply ($V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $V_L = +5\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analogue Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	4.0		Ω typ	$V_D = -10\text{ V}$ to $+10\text{ V}$, $I_S = -10\text{ mA}$
	5	7	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	$V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.5	0.5	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.2		Ω typ	$V_D = -5\text{ V}$, 0 V , $+5\text{ V}$, $I_S = -10\text{ mA}$
	0.5	0.5	Ω max	
LEAKAGE CURRENTS²				
Source OFF Leakage I_S (OFF)	± 0.02		nA typ	$V_D = \pm 10\text{ V}$, $V_S = \pm 10\text{ V}$; Test Circuit 2
	± 0.5	± 2.5	nA max	
Drain OFF Leakage I_D (OFF)	± 0.02		nA typ	$V_D = \pm 10\text{ V}$, $V_S = \pm 10\text{ V}$; Test Circuit 2
	± 0.5	± 2.5	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.04		nA typ	$V_D = V_S = \pm 10\text{ V}$; Test Circuit 3
	± 1	± 5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH} , All Others = 2.4 V or 0.8 V Respectively
		± 0.5	μA max	
DYNAMIC CHARACTERISTICS³				
t_{ON}	70		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Test Circuit 4
	180	220	ns max	
t_{OFF}	60		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Test Circuit 4
	140	180	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only)	15		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = +10\text{ V}$; Test Circuit 5
	5	5	ns min	
Charge Injection	20		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1.0\text{ nF}$; Test Circuit 6
	30		pC max	
OFF Isolation	65		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 7
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
C_S (OFF)	15		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	15		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	100		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.0001		μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital Inputs = 0 V or 5 V
	0.5	5	μA max	
I_{SS}	0.0001		μA typ	
	0.5	5	μA max	
I_L	0.0001		μA typ	
	0.5	5	μA max	
I_{GND} ³	0.0001		μA typ	
	0.5	5	μA max	

NOTES

¹Temperature range is as follows: B Version: -40°C to $+85^\circ\text{C}$.

² $T_{MAX} = +70^\circ\text{C}$.

³Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply ($V_{DD} = +12\text{ V}$, $V_{SS} = 0\text{ V}$, $V_L = +5\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	6		Ω typ	$V_D = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$
	8	10	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	$V_D = 10\text{ V}$, $I_S = -10\text{ mA}$
	0.5	0.5	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.0	1.0	Ω typ	$V_D = 0\text{ V}$, +5 V, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS^{2, 3}				
Source OFF Leakage I_S (OFF)	± 0.02		nA typ	$V_D = 0\text{ V}$, 10 V, $V_S = 0\text{ V}$, 10 V; Test Circuit 2
	± 0.5	± 2.5	nA max	
Drain OFF Leakage I_D (OFF)	± 0.02		nA typ	$V_D = 0\text{ V}$, 10 V, $V_S = 0\text{ V}$, 10 V; Test Circuit 2
	± 0.5	± 2.5	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.04		nA typ	$V_D = V_S = 0\text{ V}$, 10 V; Test Circuit 3
	± 1	± 5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.5	μA max	
DYNAMIC CHARACTERISTICS⁴				
t_{ON}	100		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +8\text{ V}$; Test Circuit 4
	220	260	ns max	
t_{OFF}	80		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = +8\text{ V}$; Test Circuit 4
	160	200	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only)	15		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = +8\text{ V}$; Test Circuit 5
	10	10	ns min	
Charge Injection	10		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1.0\text{ nF}$; Test Circuit 6
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
C_S (OFF)	15		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	15		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	100		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.0001		μA typ	$V_{DD} = +13.2\text{ V}$ Digital Inputs = 0 V or 5 V
	0.5	5	μA max	
I_L	0.0001		μA typ	
	0.5	5	μA max	$V_L = +5.5\text{ V}$
I_{GND} ⁴	0.0001		μA typ	
	0.5	5	μA max	$V_L = +5.5\text{ V}$

NOTES

¹Temperature range is as follows: B Version: -40°C to $+85^\circ\text{C}$.² $T_{MAX} = +70^\circ\text{C}$.³Tested with dual supplies.⁴Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG451/ADG452/ADG453—SPECIFICATIONS¹

Dual Supply ($V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$, $V_L = +5\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	$V_D = -3.5\text{ V}$ to $+3.5\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance (R_{ON})	7	15	Ω typ Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.3	0.5	Ω typ Ω max	$V_D = 3.5\text{ V}$, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS^{2, 3}				
Source OFF Leakage I_S (OFF)	± 0.02		nA typ	$V_D = \pm 4.5$, $V_S = \pm 4.5$; Test Circuit 2
	± 0.5	± 2.5	nA max	
Drain OFF Leakage I_D (OFF)	± 0.02		nA typ	$V_D = 0\text{ V}$, 5 V , $V_S = 0\text{ V}$, 5 V ; Test Circuit 2
	± 0.5	± 2.5	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.04		nA typ	$V_D = V_S = 0\text{ V}$, 5 V ; Test Circuit 3
	± 1	± 5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	
		± 0.5	μA max	
DYNAMIC CHARACTERISTICS⁴				
t_{ON}	160		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3\text{ V}$; Test Circuit 4
	220	300	ns max	
t_{OFF}	60		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3\text{ V}$; Test Circuit 4
	140	180	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only)	50		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = 3\text{ V}$; Test Circuit 5
	5	5	ns min	
Charge Injection	10		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1.0\text{ nF}$; Test Circuit 6
OFF Isolation	65		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 7
Channel-to-Channel Crosstalk	-76		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 8
C_S (OFF)	15		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	15		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	100		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.0001		μA typ	$V_{DD} = +5.5\text{ V}$ Digital Inputs = 0 V or 5 V
	0.5	5	μA max	
I_{SS}	0.0001		μA typ	$V_L = +5.5\text{ V}$
	0.5	5	μA max	
I_L	0.0001		μA typ	$V_L = +5.5\text{ V}$
	0.5	5	μA max	
I_{GND} ⁴	0.0001		μA typ	$V_L = +5.5\text{ V}$
	0.5	5	μA max	

NOTES

¹Temperature range is as follows: B Version: -40°C to $+85^\circ\text{C}$.

² $T_{MAX} = +70^\circ\text{C}$.

³Tested with dual supplies.

⁴Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG451/ADG452/ADG453

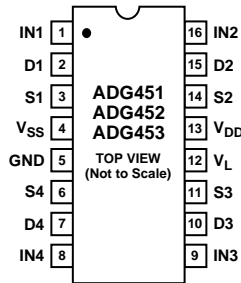
Truth Table (ADG451/ADG452)

ADG451 In	ADG452 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG453)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

**PIN CONFIGURATION
(DIP/SOIC)**



ORDERING GUIDE

Model	Temperature Range	Package Options*
ADG451BN	-40°C to +85°C	N-16
ADG451BR	-40°C to +85°C	R-16A
ADG452BN	-40°C to +85°C	N-16
ADG452BR	-40°C to +85°C	R-16A
ADG453BN	-40°C to +85°C	N-16
ADG453BR	-40°C to +85°C	R-16A

*N = Plastic DIP; R = Small Outline IC (SOIC).

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+44 V
V _{DD} to GND	-0.3 V to +25 V
V _{SS} to GND	+0.3 V to -25 V
V _L to GND	-0.3 V to V _{DD} + 0.3 V
Analog, Digital Inputs ²	V _{SS} -2 V to V _{DD} +2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA
(Pulsed at 1 ms, 10% Duty Cycle max)	
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Plastic Package, Power Dissipation	470 mW
θ _{JA} Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	+260°C

SOIC Package, Power Dissipation	600 mW
θ _{JA} Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
ESD	2 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG451/ADG452/ADG453 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

V_{DD}	Most positive power supply potential.	$V_D (V_S)$	Analog voltage on terminals D, S.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.	$C_S (OFF)$	“OFF” switch source capacitance.
V_L	Logic power supply (+5 V).	$C_D (OFF)$	“OFF” switch drain capacitance.
GND	Ground (0 V) reference.	$C_D, C_S (ON)$	“ON” switch capacitance.
S	Source terminal. May be an input or output.	t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
D	Drain terminal. May be an input or output.	t_{OFF}	Delay between applying the digital control input and the output switching off.
IN	Logic control input.	t_D	“OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
R_{ON}	Ohmic resistance between D and S.	Crosstalk	A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.
ΔR_{ON}	On resistance match between any two channels i.e., $R_{ONmax} - R_{ONmin}$.	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
$I_S (OFF)$	Source leakage current with the switch “OFF.”		
$I_D (OFF)$	Drain leakage current with the switch “OFF.”		
$I_D, I_S (ON)$	Channel leakage current with the switch “ON.”		

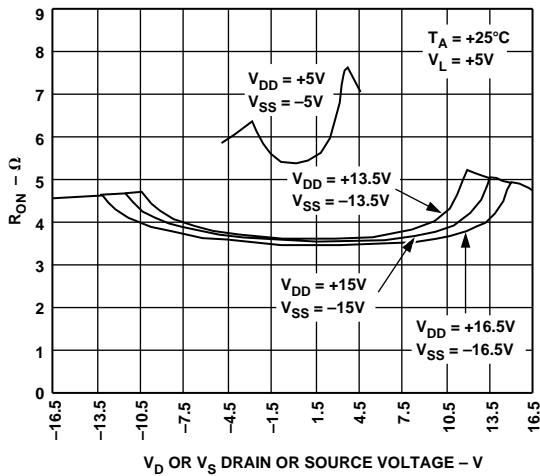


Figure 1. On Resistance as a Function of $V_D (V_S)$ for Various Dual Supplies

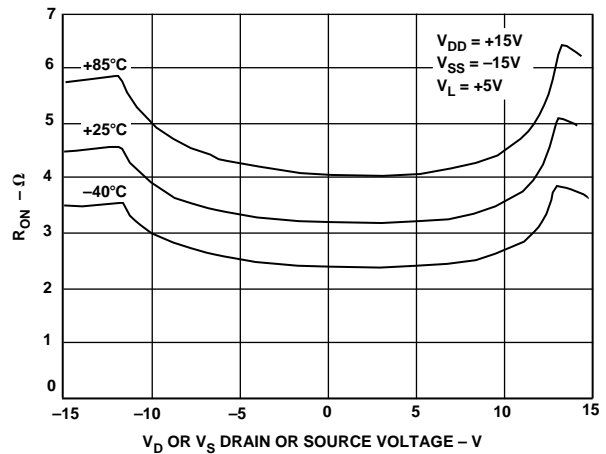


Figure 2. On Resistance as a Function of $V_D (V_S)$ for Different Temperatures with Dual Supplies

Typical Performance Characteristics—ADG451/ADG452/ADG453

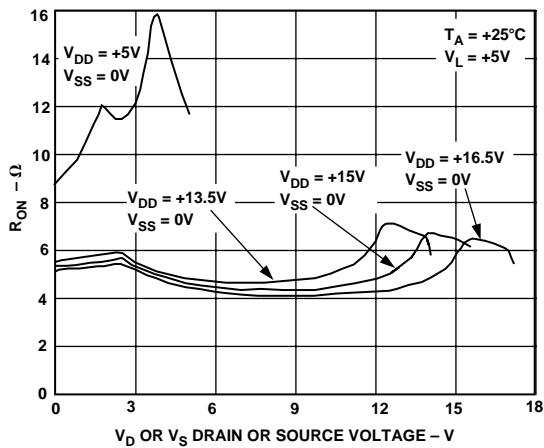


Figure 3. On Resistance as a Function of V_D (V_S) for Various Single Supplies

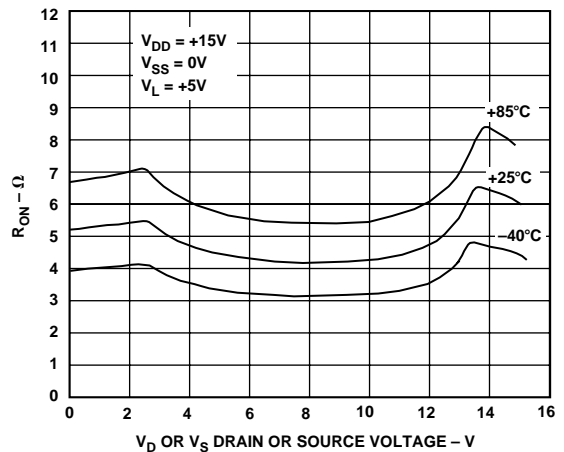


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies

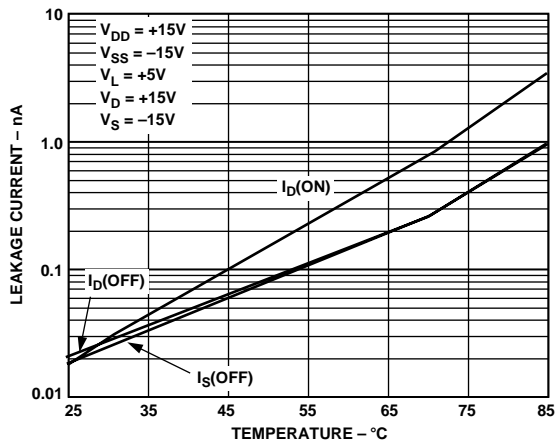


Figure 4. Leakage Currents as a Function of Temperature

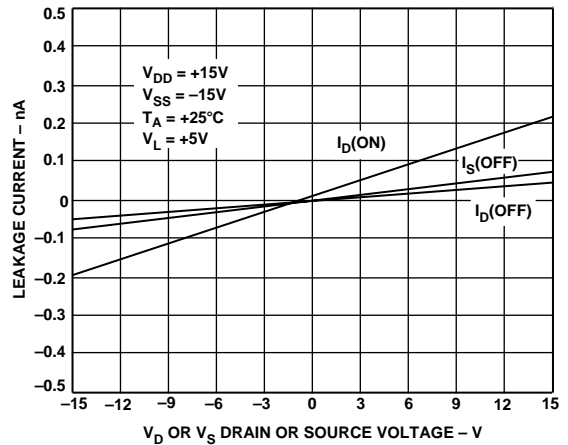


Figure 7. Leakage Currents as a Function of V_D (V_S)

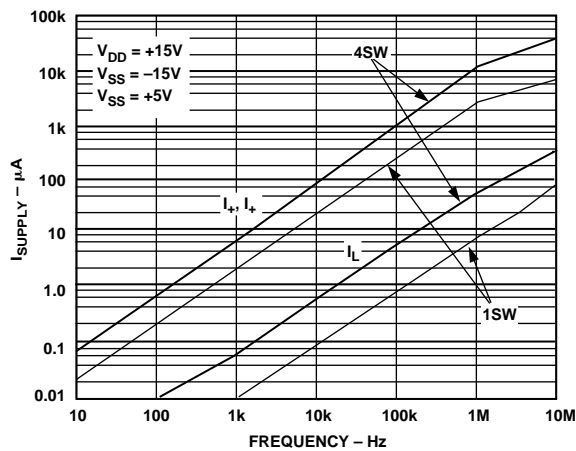


Figure 5. Supply Current vs. Input Switching Frequency

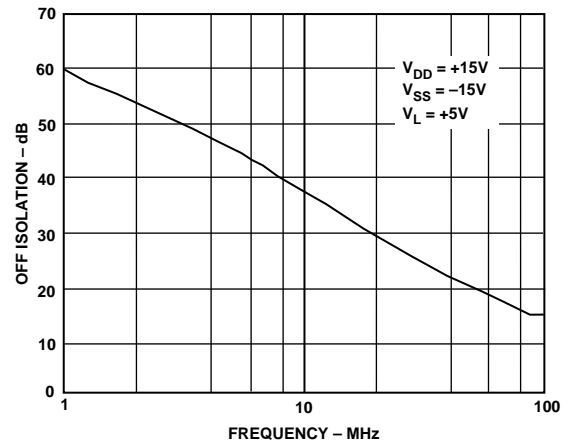


Figure 8. Off Isolation vs. Frequency

ADG451/ADG452/ADG453

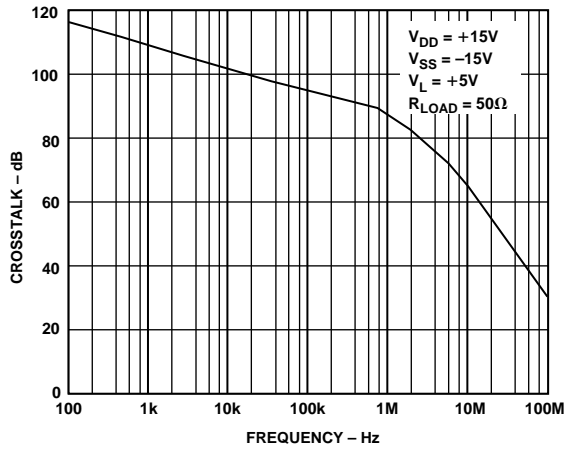


Figure 9. Crosstalk vs. Frequency

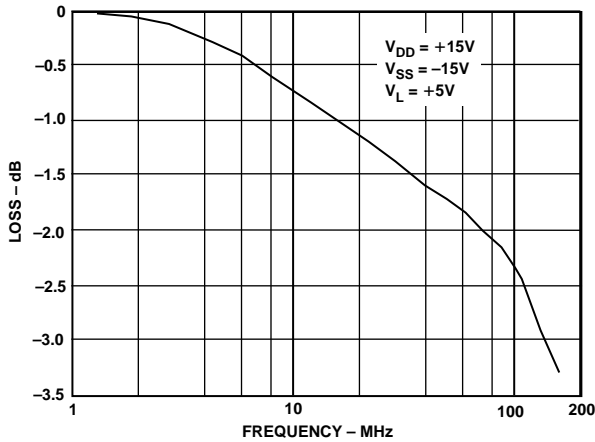


Figure 10. Frequency Response with Switch On

APPLICATION

Figure 11 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN} . In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H .

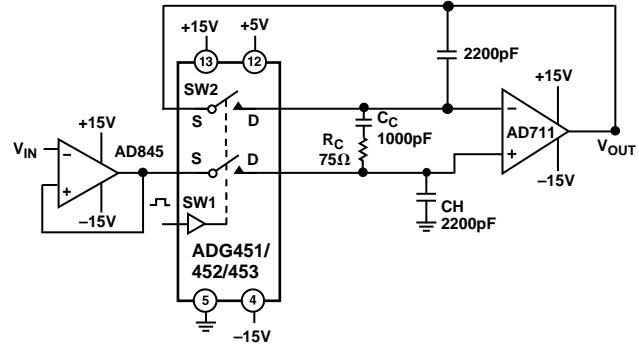
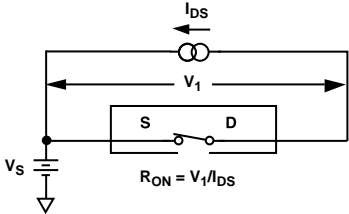


Figure 11. Fast, Accurate Sample-and-Hold Circuit

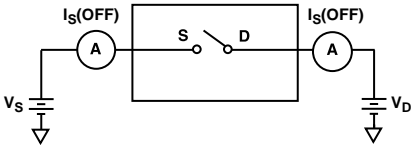
Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG451/ADG452/ADG453 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically $30 \mu\text{V}/\mu\text{s}$.

A second switch, SW2, that operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711, which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C . This compensation network reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the $\pm 10 \text{ V}$ input range. Both the acquisition and settling times are 850 ns.

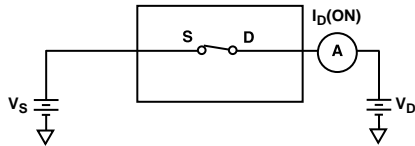
Test Circuits



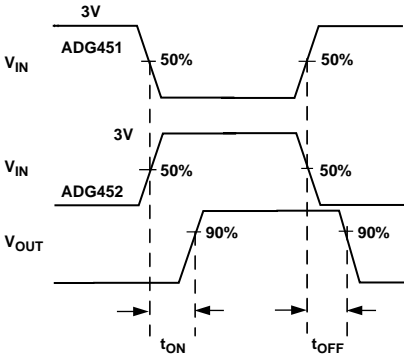
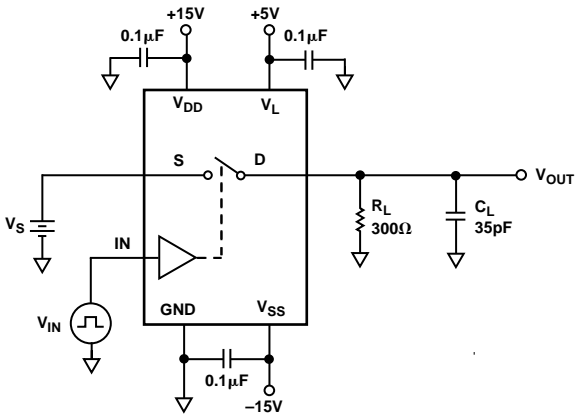
Test Circuit 1. On Resistance



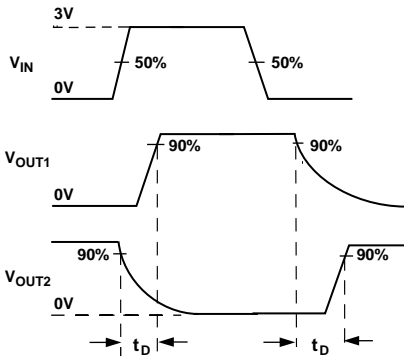
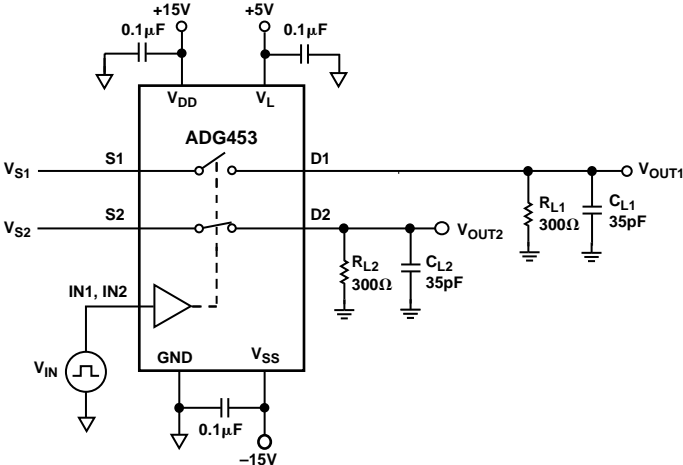
Test Circuit 2. Off Leakage



Test Circuit 3. On Leakage

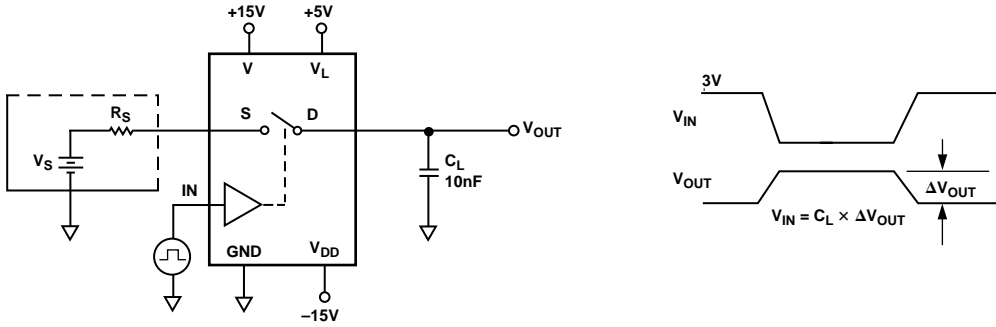


Test Circuit 4. Switching Times

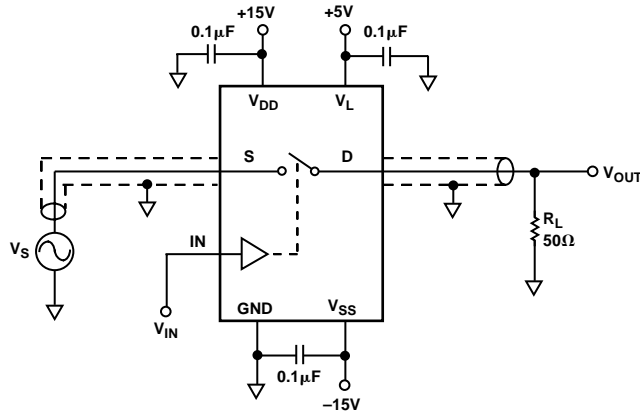


Test Circuit 5. Break-Before-Make Time Delay

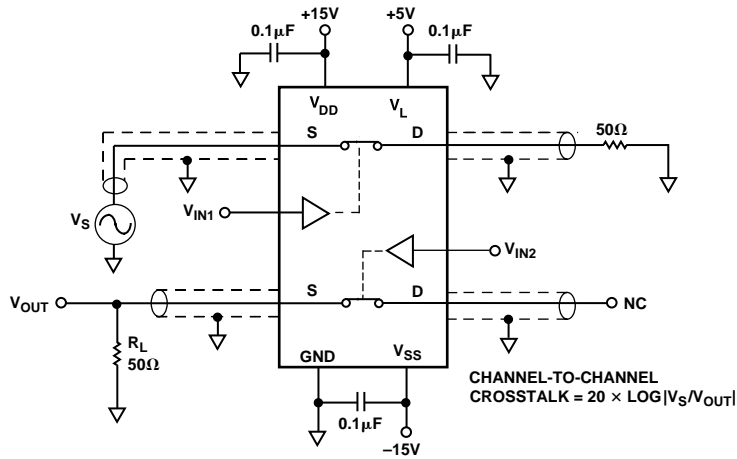
ADG451/ADG452/ADG453



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



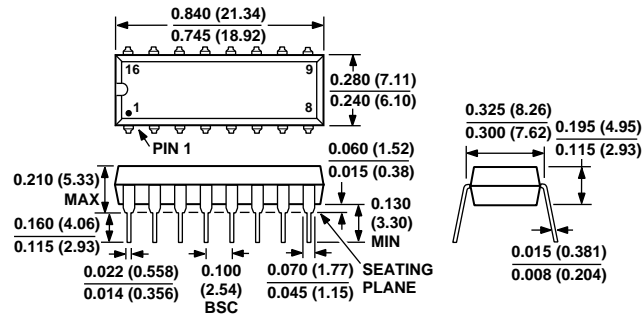
Test Circuit 8. Channel-to-Channel Crosstalk

CHANNEL-TO-CHANNEL
CROSSTALK = 20 × LOG |V_S/V_{OUT}|

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Plastic DIP (N-16)



16-Lead SOIC (R-16A)

